MX368031A
Device Test Signal Generation Software Operation Manual (For MU368030A)

Third Edition

Read this manual before using the equipment.
Keep this manual with the equipment.

Measurement Solutions

ANRITSU CORPORATION

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MX368031A
Device Test Signal Generation Software
Operation Manual (For MU368030A)

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About This Manual

This Operation Manual explains the outline, measurement examples, remote control and other aspects of MX368031A Device Test Signal Generation Software. This software is designed to be installed in the MU368030A Universal Modulation Unit mounted on the MG3680 Series Digital Modulation Signal Generator.

[ ] represents a panel key.
The MG3680 Series Digital Modulation Signal Generator Main Unit Operation Manual and the MU368030A Universal Modulation Unit Operation Manual are available as separate volumes.
Use it in conjunction with this Operation Manual.

Table of Contents

Section 1 Overview

This section describes the outline and product configuration of MX368031A Device Test Signal Generation Software product and standard accessories.

1.1 Product Overview

The MX368031A Device Test Signal Generation Software (hereinafter, referred to as this software) is system software to be installed in the MU368030A Universal Modulation Unit.
To use this software, a Universal Modulation Unit must be mounted on the MG3680 Series Digital Modulation Signal Generator.

By installing this software and selecting a Device Test Signal, you can generate modulation signals applicable to various communication systems, such as cdma2000 and GSM, without using an external baseband signal source.

1.2 Product Configuration

Standard configuration of the MX368031A is given in the table below. After unpacking, check that all items listed are included. If any items are missing or damaged, please contact Anritsu or one of our agencies.

Items	Model name/type	Product name	Quantity	Remarks
Main unit	MX368031A	Device Test Signal Generation Software	1	Supplied for Compact Flash or ATA Flash card.
Accessories		PC card adapter	1	Supplied only for Compact Flash card
	W1794AE	Operation Manual	1	

Section 2 Operation Outline

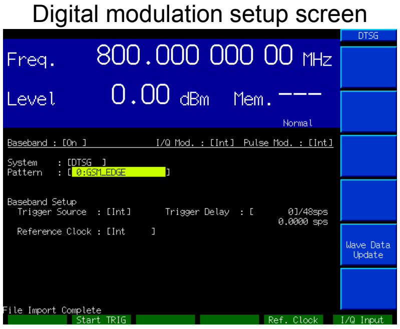
This section describes basic screen contents and how to input auxiliary signals when mounting the MU368030A Universal Modulation Unit installed with this software onto the MG3680 Series.

2.1 Screen Transitions

The screens are transited as shown below:

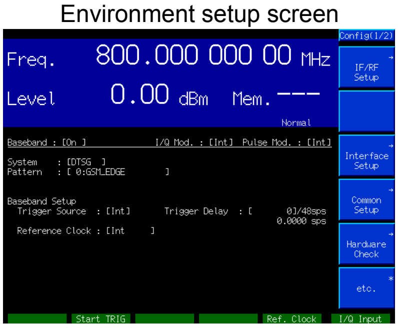
Press main function key “Digital Mod.”

Digital modulation setup screen

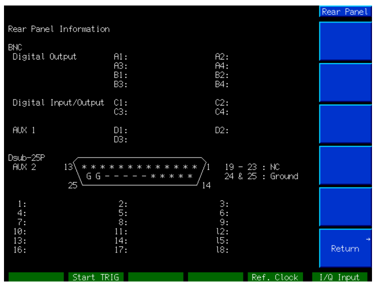


Press main function key “Config.”

Environment setup screen

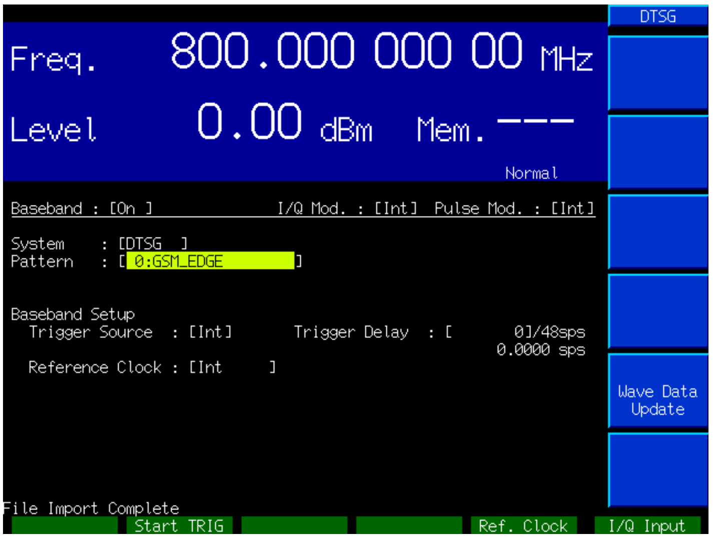


Rear Panel Information screen



2.2 Setting Modulation Parameters

Pressing Digital Mod causes the indicator LED to go on and the Main screen to appear. Basic parameters related to digital modulation can be set on this screen. This section describes settings for the Main screen.



[1] Baseband

Select On/Off for the operation of the Baseband Signal Generator Unit.

[2] I/Q Mod.

Select the I/Q signal source for orthogonal modulation. Select “Int” to use the internal signal source for the I/Q signal (using this software) or “Ext” to use the external input.

Initial value: Int

[3] Pulse Mod.

Set the modulation signal on the pulse modulator.

Int: Selects the control signal generated by this software.

Ext: Uses the external input signal for pulse modulation regardless of modulation settings.

Off: No pulse modulation

[4] System

Set the system software. Select “DTSG” to start this software.

[5] Pattern

Select the Device Test Signal.

The Device Test Signal is a modulation signal available on this software that is suitable for evaluating devices used in mobile communication system's base stations or terminals. For Device Test Signals available, refer to “Device Test Signals list” in Section 3.1.

[6] Trigger Source

Int: Outputs an RF signal in synchronization with the internal trigger signal.

Ext: Outputs an RF signal in synchronization with the trigger signal input to the Start TRIG connector. "Ext" can only be selected when a Device Test Signal applicable to "cdma2000 system Reverse" has been selected. Refer to "Device Test Signals list" in Section 3.1.

[7] Trigger Delay

It sets the output signal delay for the trigger signal input to the Start TRIG connector. For details, refer to Section 3.2.

[8] Reference Clock

Int: Generates the reference clock inside MG3681A.

Ext (TTL) : Inputs the reference clock externally (using the Ref. Clock connector). At this time, set this connector to TTL mode.

Ext (AC) : Same as Ext except that the Ref. Clock connector mode should be set to AC (5Vp-p).

2.3 Inputting External Trigger Signal

You can synchronize the signal input from Start TRIG at digital signal input connector No. 2 on the front panel of the main unit with the RF output timing. For details, refer to Section 3.2.

2.4 Re-installing data of the Universal Modulation Unit

It is available to re-install data of the Universal Modulation Unit. First, insert the attached memory card, which has MX368031A saved, into the PC-card slot on the rear panel of the MG3680 series. Then, press F5 (Wave Data Update) in the Digital Modulation Parameter Setting Screen. Selecting "yes" in the Selecting window starts downloading. It takes approximately six minutes to complete. Do not turn the power off while downloading is in progress.

Section 3 Details of Functions

This section explains the modulation signals applicable to various systems and synchronization with the external trigger input.

3.1 Modulation Signal Details

A list of Device Test Signals is given below.

Table 3-1 Device Test Signals list

No.	Device Test Signals	Applicable systems	Frame-coding	Symbol data	Synchronization with external trigger
0	GSM_EDGE	EDGE	Absent	PN9 continuous	Disabled
1	GSM_GMSK	GSM	Absent	PN9 continuous	Disabled
2	Pi/4DQPSK_PDC	PDC	Absent	PN9 continuous	Disabled
3	Pi/4DQPSK_IS-136	IS-136	Absent	PN9 continuous	Disabled
4	Pi/4DQPSK_PHS	PHS	Absent	PN9 continuous	Disabled
5	1xRTTrc1_RVS	cdmaOne/2000 1xRTT RC1 Reverse	Present	FCH 9.6kbps	Enabled
6	1xRTTrc3(1)_RVS	cdma2000 1xRTT RC3 Reverse	Present	PICH FCH 9.6kbps	Enabled
7	1xRTTrc3(2)_RVS	cdma2000 1xRTT RC3 Reverse	Present	PICH FCH 9.6kbps SCH 9.6kbps	Enabled
8	1xRTTrc3(3)_RVS	cdma2000 1xRTT RC3 Reverse	Present	PICH DCCH 9.6kbps	Enabled
9	1xRTTrc1-2_FWD	cdmaOne/2000 1xRTT RC1-2 Forward	Spreading only	PICH、SyncCH、PagingCH FCH 19.2ksps x 6	Disabled
10	1xRTTrc3-5_FWD	cdma2000 1xRTT RC3-5 Forward	Spreading only	PICH、SyncCH、PagingCH FCH 38.4ksps x 6	Disabled
11	1xEV-DO_FWD	cdma2000 1xEV-DO Forward 16QAM	Spreading only	Traffic Channel	Disabled
12	1xEV-DO_RVS	cdma2000 1xEV-DO Reverse	Spreading only	Traffic Channel	Disabled

3.1.1 EDGE System (GSM_EDGE)

When this Device Test Signal is selected, the PN9-stage pseudo-random pattern 511-bit circulating data is modulated to 3π/8offset 8PSK with a Gaussian linear filter and output. The PN9-stage pseudo-random pattern used as data has continuity. The symbol rate is 273.833··· ksps.

3.1.2 GSM System (GSM_GMSK)

When this Device Test Signal is selected, the PN9-stage pseudo-random pattern 511-bit circulating data is GMSK-modulated and output. The PN9-stage pseudo-random pattern used as data has continuity. The symbol rate is 273.833··· ksps.

3.1.3 PDC System (Pi/4DQPSK_PDC)

When this Device Test Signal is selected, the PN9-stage pseudo-random pattern 511-bit circulating data is modulated to π/4DQPSK with a Root Nyquist filter (α=0.5) and output. The PN9-stage pseudo-random pattern used as data has continuity. The symbol rate is 21 ksps.

3.1.4 IS-136 system (Pi/4DQPSK_IS-136)

When this Device Test Signal is selected, the PN9-stage pseudo-random pattern 511-bit circulating data is modulated to π/4DQPSK with a Root Nyquist filter (α=0.35) and output. The PN9-stage pseudo-random pattern used as data has continuity. The symbol rate is 24.3 ksps.

3.1.5 PHS system (Pi/4DQPSK_PHS)

When this Device Test Signal is selected, the PN9-stage pseudo-random pattern 511-bit circulating data is modulated to π/4DQPSK with a Root Nyquist filter (α=0.5) and output. The PN9-stage pseudo-random pattern used as data has continuity. The symbol rate is 192 ksps.

3.1.6 cdma2000 system

3.1.6.1 1xRTT Reverse RC1 (1xRTTrc1_RVS)

When this Device Test Signal is selected, R-FCH of 1xRTT Reverse RC1 is output. Frame-coding and IQ modulation are carried out according to 3GPP2 C.S0002-0-2. The output signal parameter is given below.

	Data Rate	Data
R-FCH	9.6 kbps	PN9fix*

R-FCH(Reverse Fundamental Channel)

Frame-coding shown in the functional block diagram given below is carried out for the signals output by selecting this Device Test Signal. Frame-coding is carried out for four continuous frames (taking 20 ms to output one frame) and a 4-frame length waveform pattern obtained by frame-coding is repeatedly output. Because the length of the three cycles of I/Q channel PN sequence used for short-code spreading equal the 4-frame length, the short code keeps continuity during outputting the signal. Therefore, this output signal can be used for modulation accuracy measurement or Frame Error Rate (FER) measurement using CRC. No spreading is made using long code.

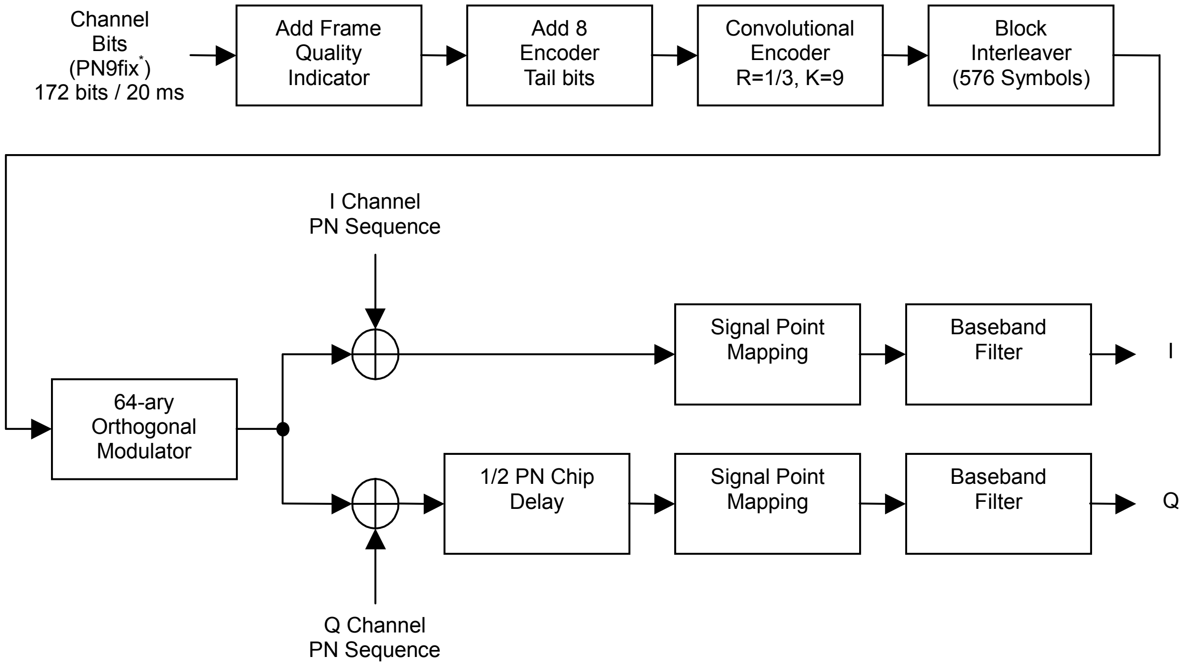


Fig. 3-1 Device Test Signal–Block diagram of 1xRTTrc1_RVS

* As shown in the following figure, the PN9 generator is initialized every four frames and the same 4-frame length data is repeatedly output. Therefore, PN9fix keeps continuity within these four frames but not with other sets of four frames.

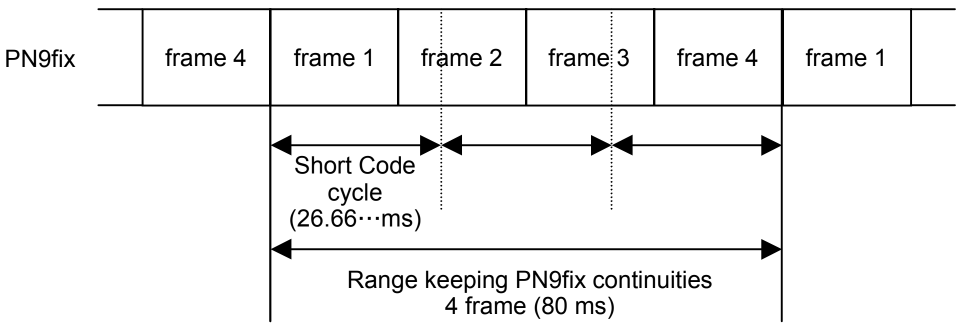


Fig. 3-2 PN9fix data and short code

3.1.6.2 1xRTT Reverse RC3 (1xRTTrc3(1)_RVS)

When this Device Test Signal is selected, 1xRTT Reverse RC3 multiple signal is output. Frame-coding and IQ modulation are carried out according to 3GPP2 C.S0002-0-2. The multiplexed channels are PICH and R-FCH. The parameters for multiplexed channels are given below.

	Walsh Code	Code Power	Data Rate	Data
R-PICH	0	–5.278 dB	N/A	All “0”
R-FCH	4	–1.528 dB	9.6 kbps	PN9fix*

R-PICH (Reverse Pilot Channel),
R-FCH (Reverse Fundamental Channel)

Frame-coding shown in the functional block diagram given below is carried out for signals output by selecting this Device Test Signal. Frame-coding is carried out for four continuous frames (taking 20 ms to output one frame) and a 4-frame length waveform pattern obtained by frame-coding is repeatedly output. Because the length of the three cycles of I/Q channel PN sequence used for short-code spreading equal the 4-frame length, the short code keeps continuity during outputting the signal. Therefore, this output signal can be used for modulation accuracy measurement or Frame Error Rate (FER) measurement using CRC. No spreading is made using long code.

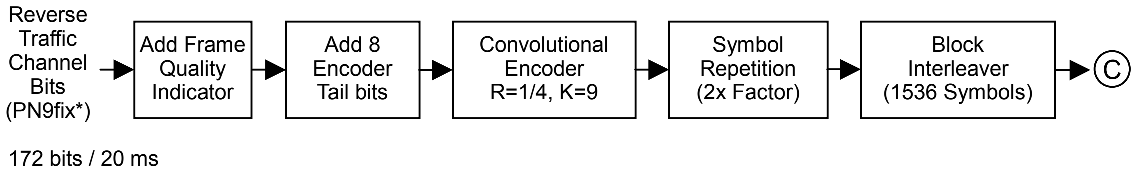
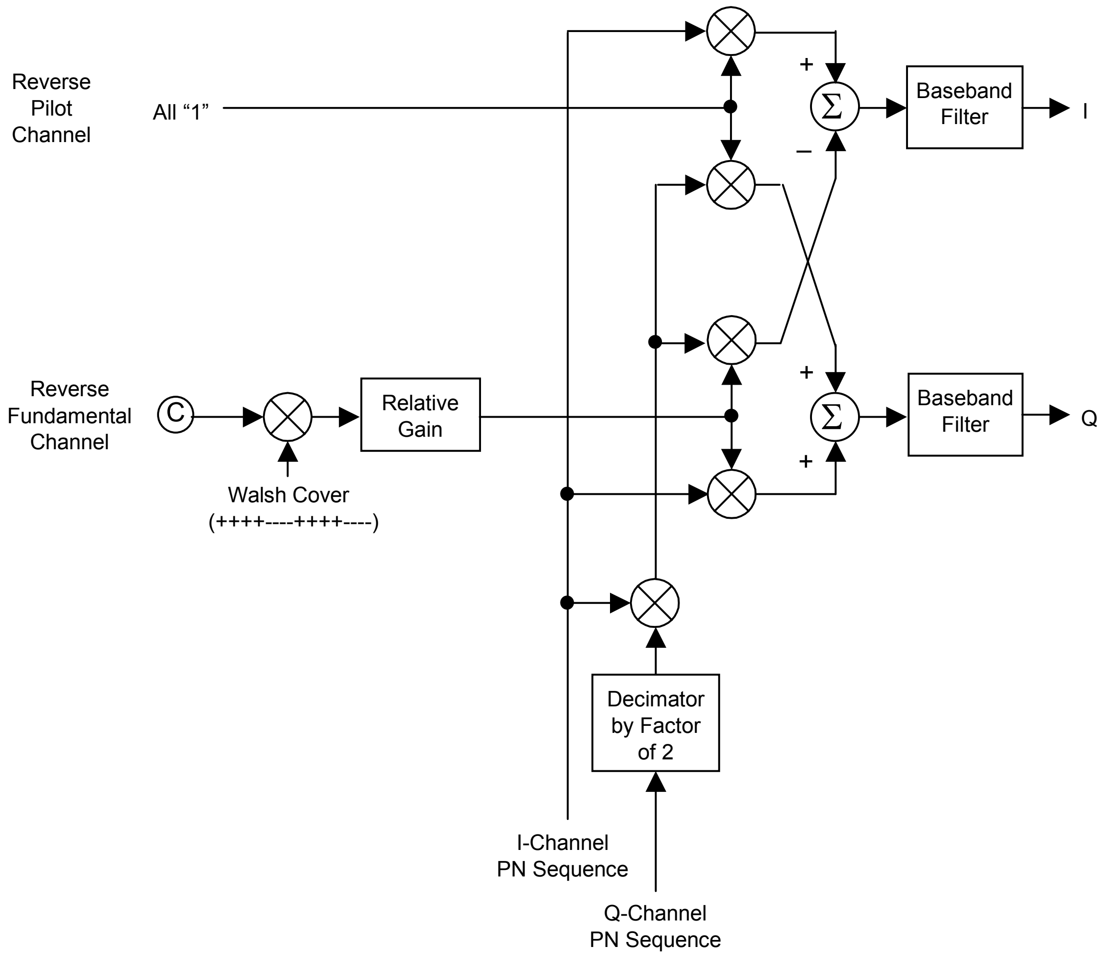


Fig. 3-3 Device Test Signal–Block diagram of 1xRTTrc3(1)_RVS (Part1/2)



Note:

Binary signal "0" is replaced with 1 and "1" with –1.

Fig. 3-4 Device Test Signal–Block diagram of 1xRTTrc3(1)_RVS (Part2/2)

* Because the PN9 generator is initialized every four frames, the same 4-frame length data is repeatedly output. Therefore, the PN9 keeps continuity within these four frames but not with other sets of four frames. See Figure "PN9fix data and short code" in Section 3.1.6.1.

3.1.6.3 1xRTT Reverse RC3 (1xRTTrc3(2)_RVS)

When this Device Test Signal is selected, 1xRTT Reverse RC3 multiple signal is output. Frame-coding and IQ modulation are carried out according to 3GPP2 C.S0002-0-2. The multiplexed channels are R-PICH, R-FCH, and R-SCH. The parameters for multiplexed channels are given below.

	Walsh Code	Code Power	Data Rate	Data
R-PICH	0	–7.5912 dB	N/A	All “0”
R-FCH	4	–3.8412 dB	9.6 kbps	PN9fix*
R-SCH	2	–3.8412 dB	9.6 kbps	PN9fix*

R-PICH (Reverse Pilot Channel),
R-FCH (Reverse Fundamental Channel),
R-SCH (Reverse Supplemental Channel)

Frame-coding shown in the functional block diagram given below is carried out for signals output by selecting this Device Test Signal. Frame-coding is carried out for four continuous frames (taking 20 ms to output one frame) and a 4-frame length waveform pattern obtained by frame-coding is repeatedly output. Because the length of the three cycles of I/Q channel PN sequence used for short-code spreading equal the 4-frame length, the short code keeps continuity during outputting the signal. Therefore, this output signal can be used for modulation accuracy measurement or Frame Error Rate (FER) measurement using CRC. No spreading is made using long code.

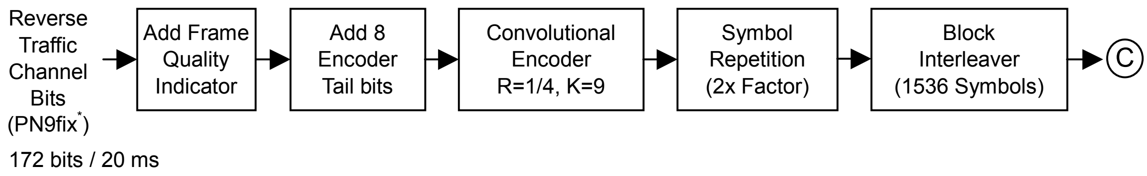
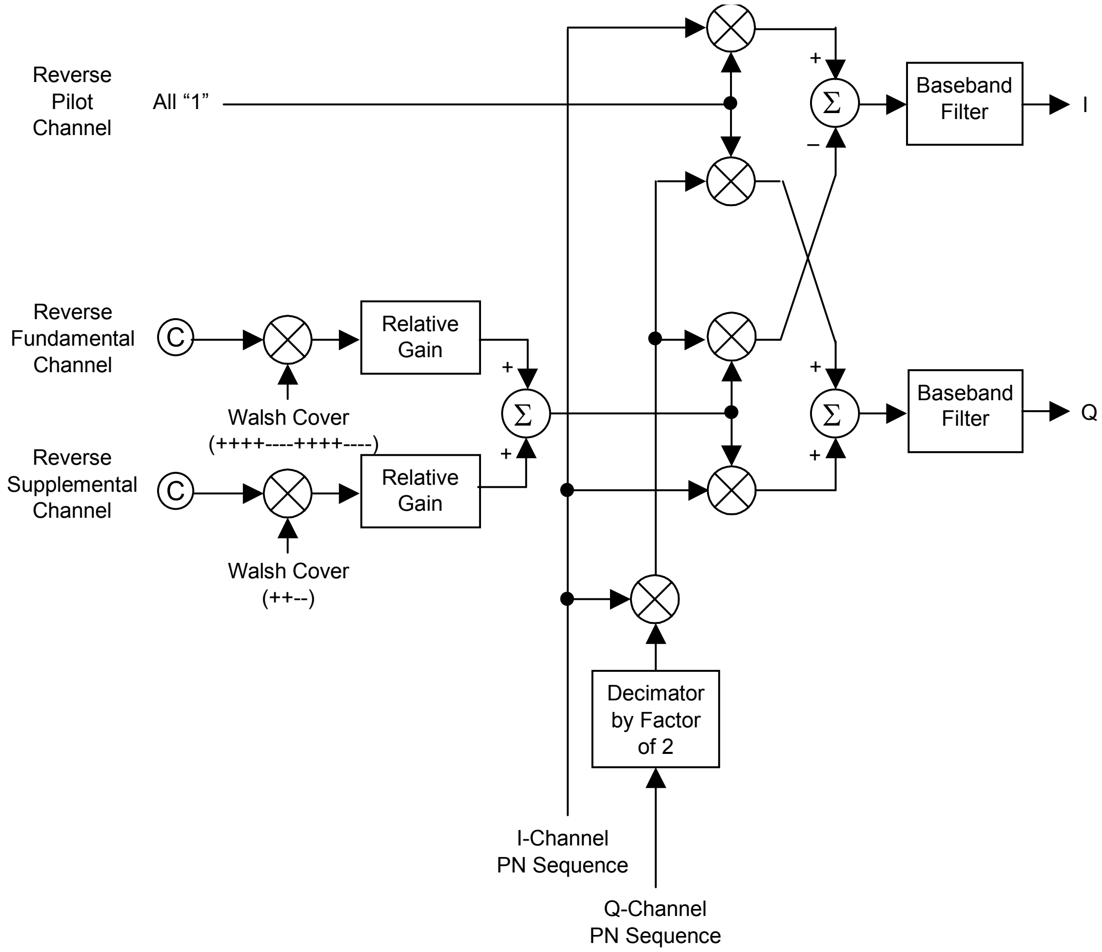


Fig. 3-5 Device Test Signal–Block diagram of 1xRTTrc3(2)_RVS (Part1/2)



Note:

Binary signal "0" is replaced with 1 and "1" with –1.

Fig. 3-6 Device Test Signal–Block diagram of 1xRTTrc3(2)_RVS (Part2/2)

* Because the PN9 generator is initialized every four frames, the same 4-frame length data is repeatedly output. Therefore, the PN9 keeps continuity within these four frames but not with other sets of four frames. See Figure "PN9fix data and short code" in Section 3.1.6.1.

3.1.6.4 1xRTT Reverse RC3 (1xRTTrc3(3)_RVS)

When this Device Test Signal is selected, 1xRTT Reverse RC3 multiple signal is output. Frame-coding and IQ modulation are carried out according to 3GPP2 C.S0002-0-2. The multiplexed channels are R-PICH and R-DCCH. The parameters for multiplexed channels are given below.

	Walsh Code	Code Power	Data Rate	Data
R-PICH	0	–5.278 dB	N/A	All "0"
R-DCCH	8	–1.528 dB	9.6 kbps	PN9fix*

R-PICH (Reverse Pilot Channel),
R-DCCH (Reverse Dedicated Channel)

Frame-coding shown in the functional block diagram given below is carried out for signals output by selecting this Device Test Signal. Frame-coding is carried out for four continuous frames (taking 20 ms to output one frame) and a 4-frame length waveform pattern obtained by frame-coding is repeatedly output. Because the length of the three cycles of I/Q channel PN sequence used for short-code spreading equal the 4-frame length, the short code keeps continuity during outputting the signal. Therefore, this output signal can be used for modulation accuracy measurement or Frame Error Rate (FER) measurement using CRC. No spreading is made using long code.

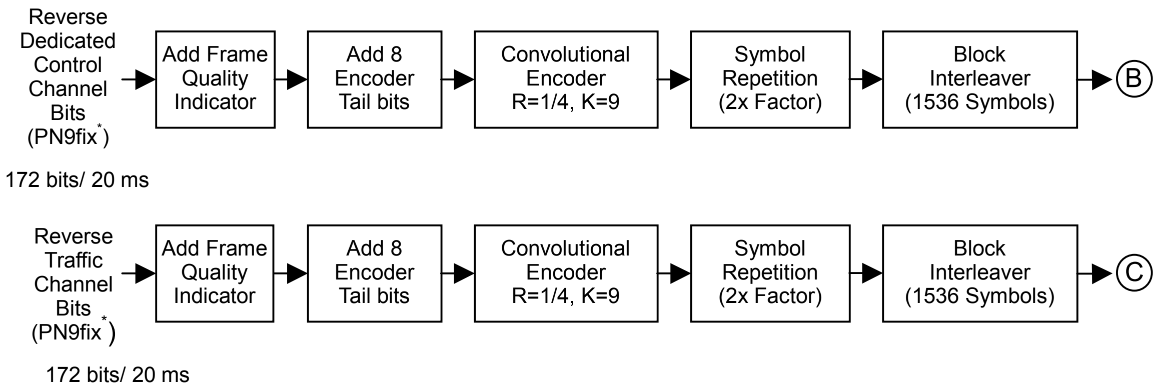
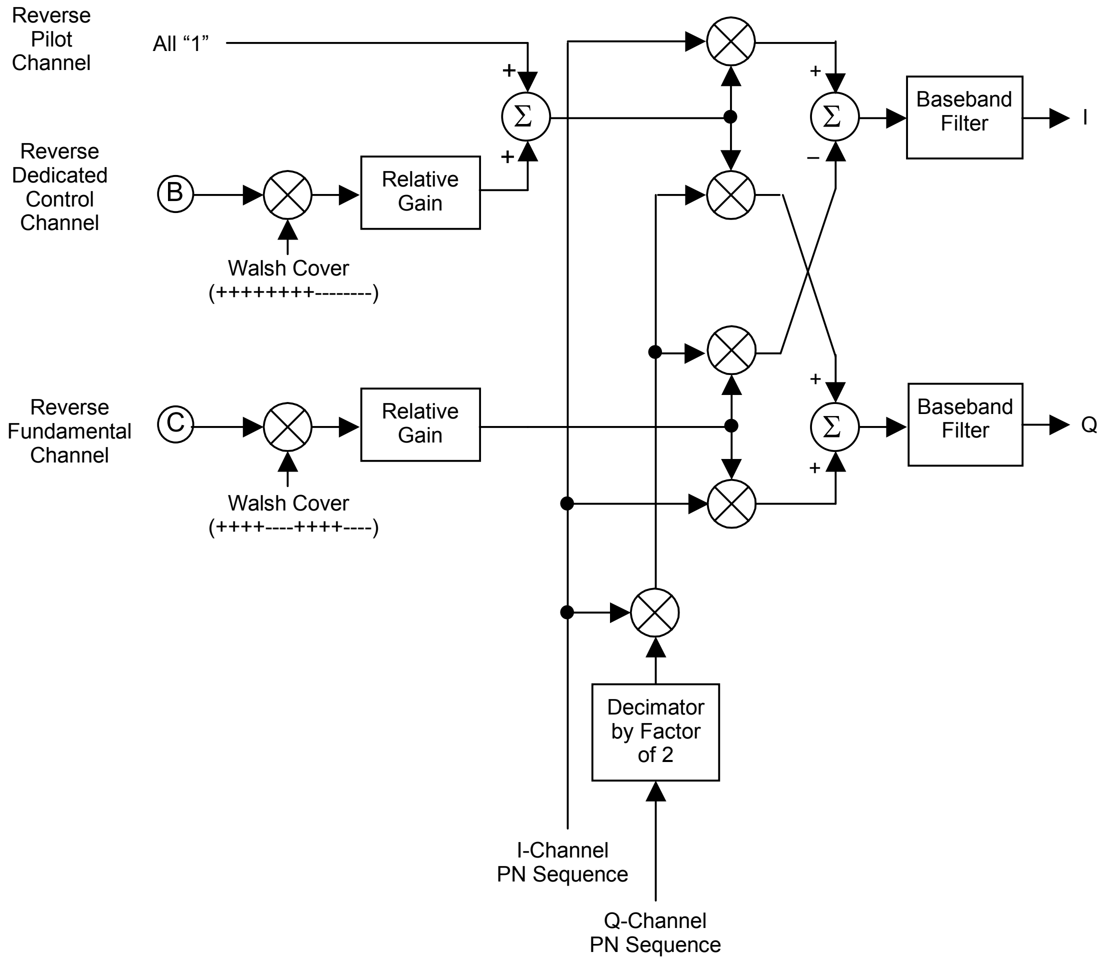


Fig. 3-7 Device Test Signal–Block diagram of 1xRTTrc3(3)_RVS (Part1/2)



Note:

Binary signal "0" is replaced with 1 and "1" with –1.

Fig. 3-8 Device Test Signal–Block diagram of 1xRTTrc3(3)_RVS (Part2/2)

* Because the PN9 generator is initialized every four frames and the same 4-frame length data is repeatedly output. Therefore, the PN9 keeps continuity within these four frames but not with other sets of four frames. See Figure "PN9fix data and short code" in Section 3.1.6.1.

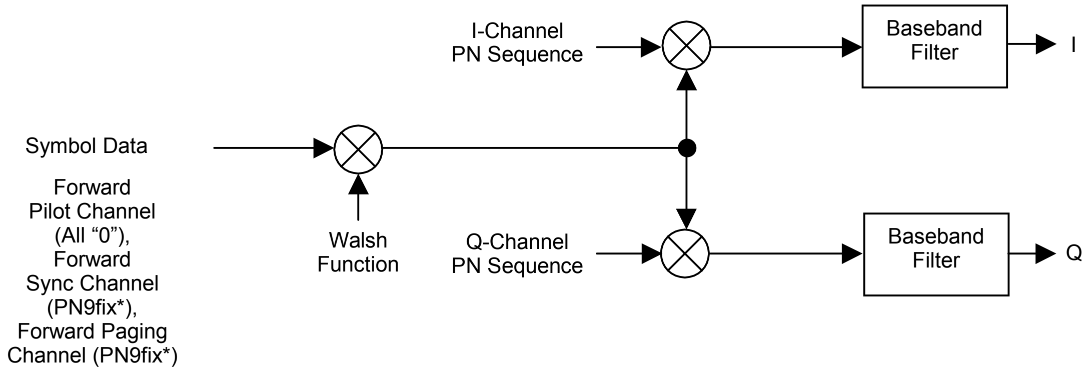
3.1.6.5 1xRTT Forward RC1 (1xRTTrc1-2_FWD)

When this Device Test Signal is selected, 1xRTT Forward RC1 multiple signal is output according to 3GPP2 C.S0002-0-2. The multiplexed channels are F-PICH, F-SyncCH, PagingCH, and F-FCHx6 (data sequences obtained by spreading six symbol data sequences with Walsh code 8, 9, ···, and 13). The parameters for multiplexed channels are given below.

	Walsh Code	Code Power	Symbol Rate	Symbol Data
F-PICH	0	–7.0 dB	N/A	All “0”
F-SyncCH	32	–13.3 dB	4.8 ksps	PN9fix*
PagingCH	1	–7.3 dB	19.2 ksps	PN9fix*
F-FCH x 6	8 to 13	–10.3 dB	19.2 kbps	PN9fix*

F-PICH (Forward Pilot Channel), F-SyncCH (Forward Sync Channel), PagingCH (Paging Channel), F-FCH (Forward Fundamental Channel)

Processing shown in the following functional block diagram is carried out for the signals output by selecting this Device Test Signal. This functional block diagram shows functional blocks for individual channels and symbol data for each channel is added after being processed as shown in this functional block diagram. This processing is carried out for four continuous frames (taking 20 ms to output one frame) and a 4-frame length waveform pattern obtained as a result of this processing is repeatedly output. Because the length of the three cycles of I/Q channel PN sequence used for short-code spreading equal the 4-frame length, the short code keeps continuity during outputting the signal. Therefore, this output signal can be used for modulation accuracy measurement. Scrambling with long code and PCB Mux are not carried out.



Note:

Binary signal "0" is replaced with 1 and "1" with –1.

Fig. 3-9 Device Test Signal–Block diagram of 1xRTTrc1-2_FWD

* Because the PN9 generator is initialized every four frames and the same 4-frame length data is repeatedly output. Therefore, the PN9 keeps continuity within these four frames but not with other sets of four frames. See Figure "PN9fix data and short code" in Section 3.1.6.1.

3.1.6.6 1xRTT Forward RC3 (1xRTTrc3-5_FWD)

When this Device Test Signal is selected, 1xRTT Forward RC3 multiple signal is output according to 3GPP2 C.S0002-0-2. The multiplexed channels are F-PICH, F-SyncCH, PagingCH, and F-FCHx6 (six data sequences obtained by spreading six symbol data sequences with Walsh code 8, 9, ···, and 13). The parameters for multiplexed channels are given below.

	Walsh Code	Code Power	Symbol Rate	Symbol Data
F-PICH	0	–7.0 dB	N/A	All “0”
F-SyncCH	32	–13.3 dB	4.8 ksps	PN9fix*
PagingCH	1	–7.3 dB	19.2 ksps	PN9fix*
F-FCH x 6	8 to 13	–10.3 dB	38.4 kbps	PN9fix*

F-PICH (Forward Pilot Channel), F-SyncCH (Forward Sync Channel), PagingCH (Paging Channel), F-FCH (Forward Fundamental Channel)

Processing shown in the functional block diagram given below is carried out for the signals output by selecting this Device Test Signal. This functional block diagram shows functional blocks for individual channels and symbol data for each channel is added after being processed as shown in this functional block diagram. This processing is carried out for four continuous frames (taking 20 ms to output one frame) and a 4-frame length waveform pattern obtained as a result of this processing is repeatedly output. Because the length of the three cycles of I/Q channel PN sequence used for short-code spreading equal the 4-frame length, the short code keeps continuity during outputting the signal. Therefore, this output signal can be used for modulation accuracy measurement. Scrambling with long code and PCB Mux arse not carried out.

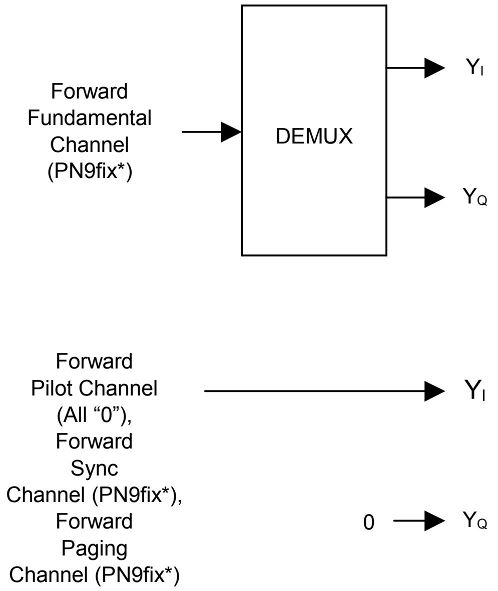
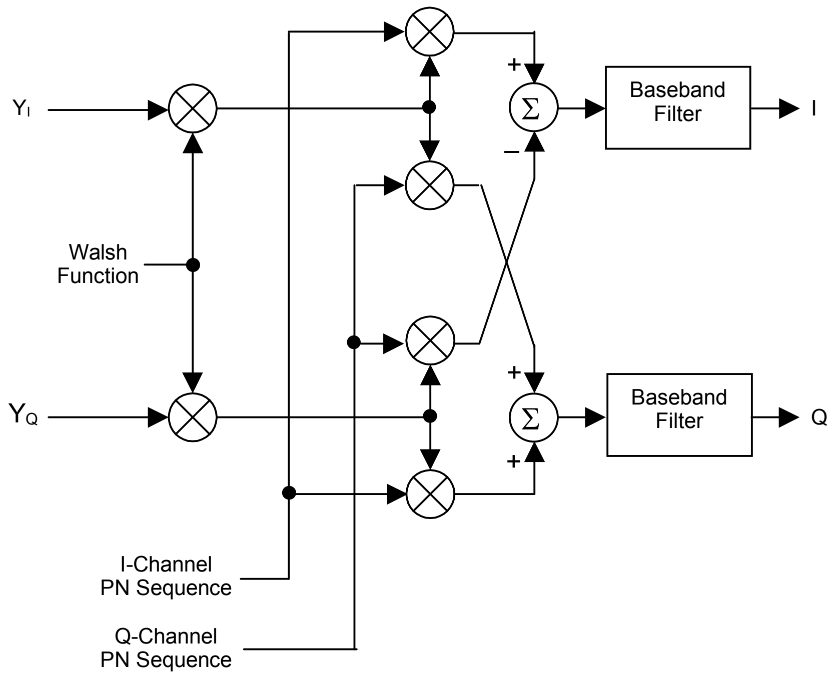


Fig. 3-10 Device Test Signal–Block diagram of 1xRTTrc3-5_FWD (Part1/2)



Note:

Binary signal "0" is replaced with 1 and "1" with –1.

* Because the PN9 generator is initialized every four frames and the same 4-frame length data is repeatedly output. Therefore, the PN9 keeps continuity within these four frames but not with other sets of four frames. See Figure "PN9fix data and short code" in Section 3.1.6.1.

Fig. 3-11 Device Test Signal–Block diagram of 1xRTTrc3-5_FWD (Part2/2)

3.1.6.7 1xEV-DO Forward (1xEV-DO_FWD)

When this Device Test Signal is selected, 1xEV-DO Forward multiple signal is output according to 3GPP2 C.S0024. The multiplexed channels are given in the table below. For F-TCH, no channel coding is carried out; PN15fix* data is directly modulated with 16 QAM.

		MAC index	Power	Data	Notes
Preamble		5	0.0 dB	All “0”	
Pilot Channel		N/A	0.0 dB	All “0”	
MAC Channel	RPC	5	–3.0 dB	All “0”	
	RA	N/A	–3.0 dB	All “0”	
Traffic Channel		N/A	0.0 dB	PN15fix*	16 QAM 1536 Symbol/slot

The block diagrams for IQ mapping and time division multiplex (TDM) follow.

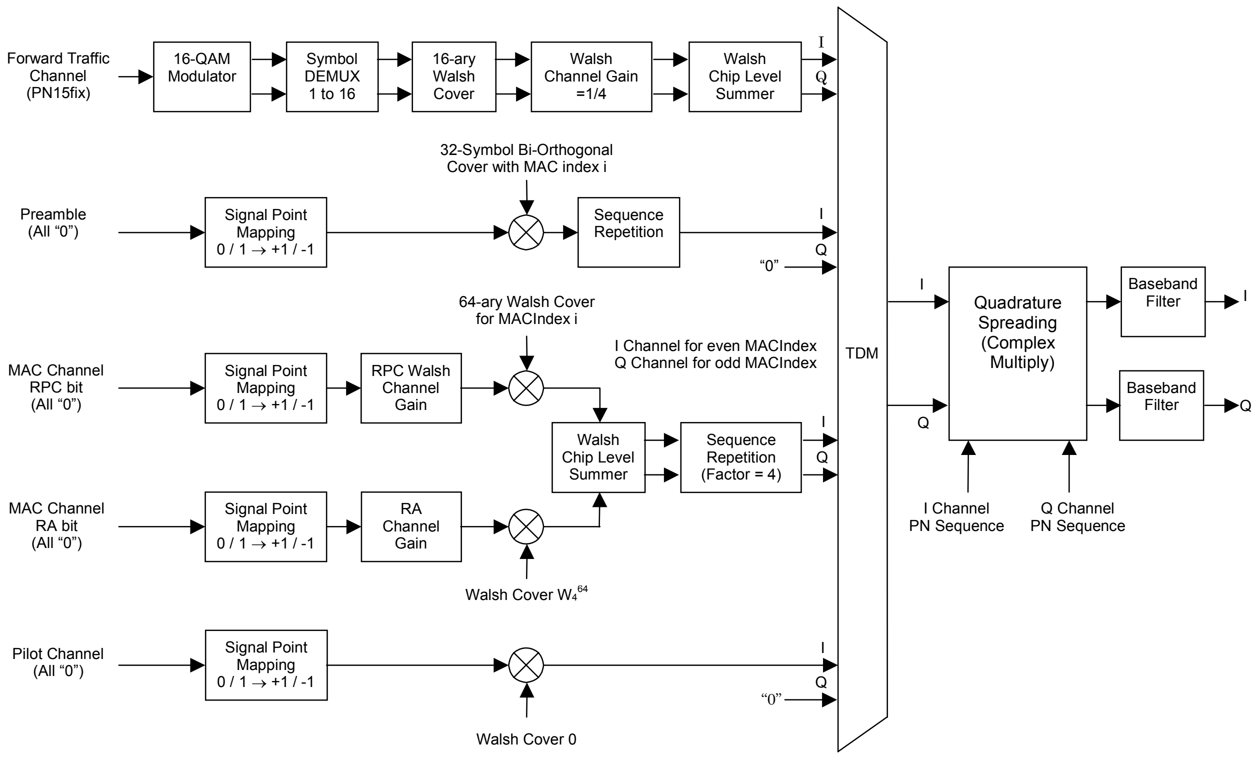


Fig. 3-12 Device Test Signal–Block diagram of 1xEV-DO_FWD (Part1/2)

Preamble	Data	MAC	Pilot	MAC	Data	MAC	Pilot	MAC	Data
64 chip	336 chip	64 chip	96 chip	64 chip	800 chip	64 chip	96 chip	64 chip	400 chip

1 slot = 1.67 ms

Fig. 3-13 Device Test Signal–Block diagram of 1xEV-DO_FWD (Part2/2)

* Because the PN15 generator is initialized every three frames, the same 3-frame length data is repeatedly output. Therefore, the PN15 keeps continuity within these three frames but not with other sets of three frames.

3.1.6.8 1xEV-DO Reverse (1xEV-DO_RVS)

When this Device Test Signal is selected, 1xEV-DO Reverse multiple signal is output according to 3GPP2 C.S0024. The multiplexed channels are given in the table below.

	Walsh Code	Power	Data	Notes
Pilot Channel	0	–18.68 dB	All "0"	
RRI Channel	0	–18.68 dB	RRI Symbol = "101"	
DRC Channel	0 (8-ary Walsh Func.) & 8	–18.68 dB	DRC Value = "0x01"	
ACK Channel	4	–18.68 dB	All "0"	
Reverse Data Channel	2	–0.18 dB	PN9fix*	8192 Symbol/slot

Processing shown in the functional block diagram given below is carried out for signals output by selecting this Device Test Signal. For reverse data channels, no channel coding is carried out; PN9fix* data is directly spread. The DRC and ACK channels are active at all time slots. This processing is carried out for three continuous frames (taking 26.66··· ms to output one frame) and a 3-frame length waveform pattern obtained as a result of this processing is repeatedly output.
As the long code mask, 0x3FFFFFFFFFF is used for MI and 0x00000000001 for MQ.

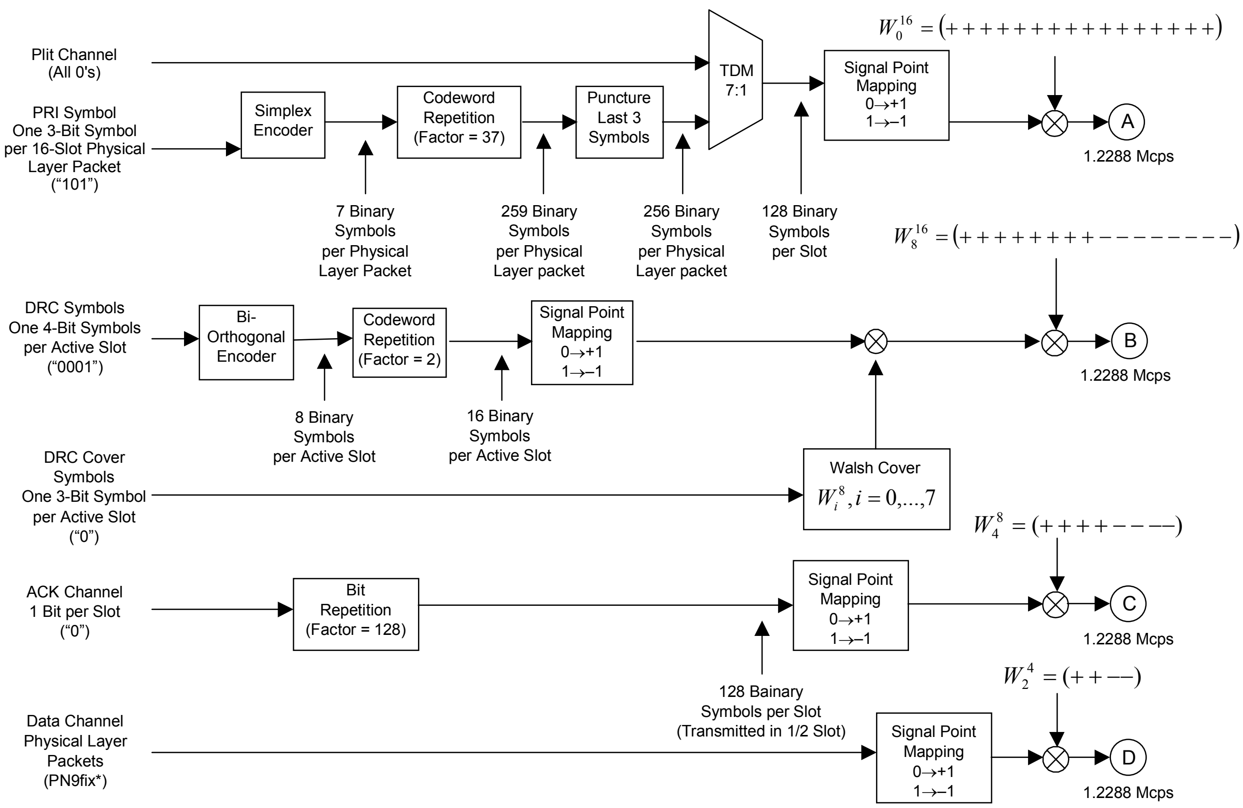


Fig. 3-14 Device Test Signal–Block diagram of 1xEV-DO_RVS (Part1/2)

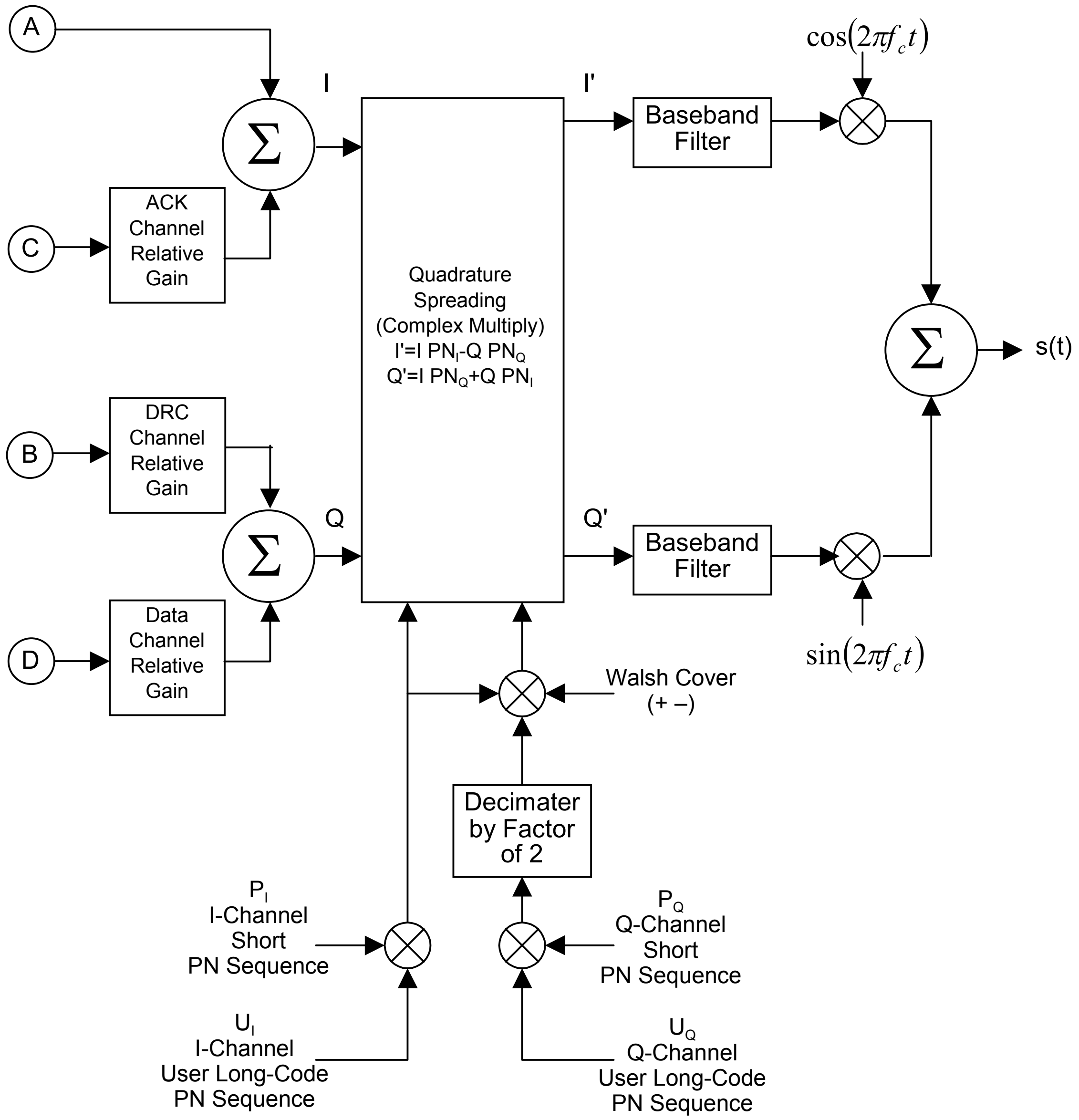


Fig. 3-15 Device Test Signal–Block diagram of 1xEV-DO_RVS (Part2/2)

* Because the PN9 generator is initialized every three frames, the same 3-frame length data is repeatedly output. Therefore, the PN9 keeps continuity within these three frames but not with other sets of three frames.

3.2 External Trigger

The figure given below shows the RF signal output timing for inputting a trigger signal to the Start TRIG input (front panel) for synchronizing with other devices. This external trigger operation can be set only when a Device Test Signal applicable to cdma2000 1xRTT Reverse has been selected. The RF signal is output with a delay of 9/8 chip (1 chip = 1/1228.8 ms) plus trigger delay set value from the trigger rise edge. Because the RF output timing includes an error of ±2/16 chip, the actual delay from Start TRIG input is as shown in the expression given below.

(Delay from Start TRIG input) =
9/8 chip + (Trigger Delay) ± (Delay error)

START TRIG input is TTL.

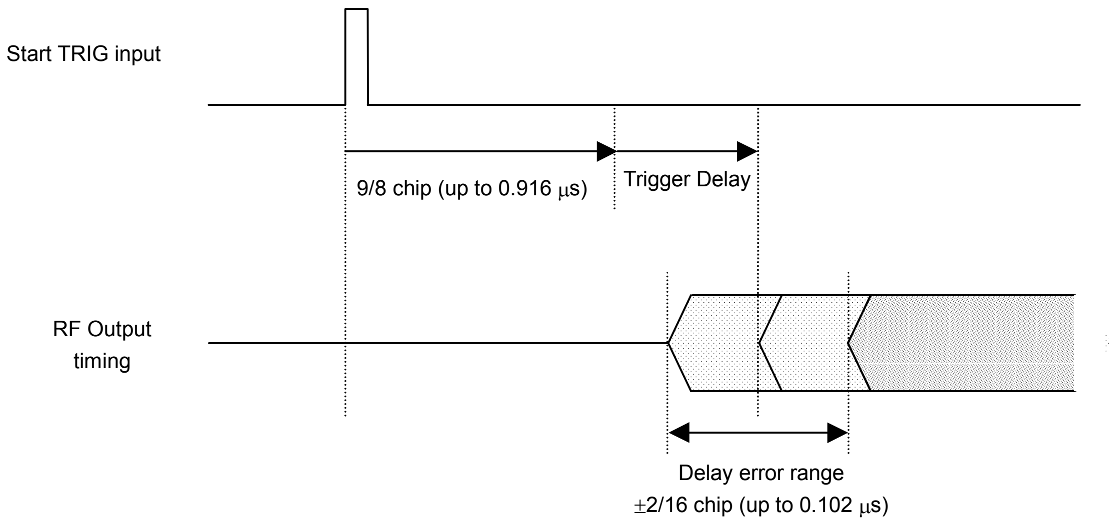


Fig. 3-16 External trigger operation

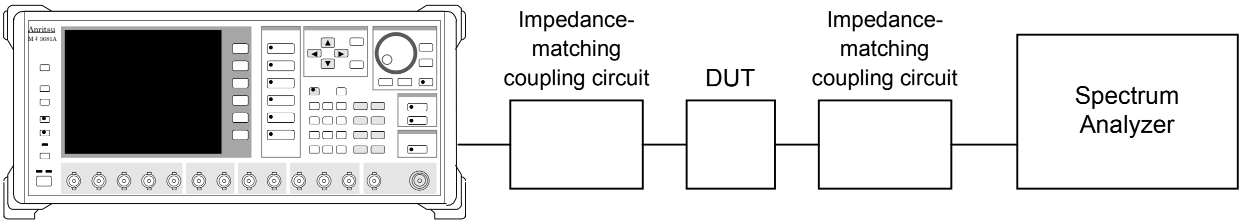
Section 4 Measurement

This section explains transmission amplifier evaluation measurement, as an example of measurement when mounting the MU368030A Universal Modulation Unit installed with the MX368031A Device Test Signal Generation Software onto the MG3681A Digital Modulation Signal Generator.

4.1 Evaluation Measurement of the Transmission Amplifier's Adjacent Channel Leakage Power Ratio

This section explains evaluation measurement of the Adjacent Channel Leakage Power Ratio on the Transmission Amplifier.

Setup



Measurement procedure

[1] Set the MG3681A frequency to the one used for the test.

[2] Set the MG3681A output level to one suitable for the DUT and Impedance-matching coupling circuit.

[3] Set the Device Test Signal to be measured in the MG3681A Pattern.

[4] Use a spectrum analyzer to evaluate the adjacent channel leakage power ratio.

Section 5 Remote Control

This section provides a list of GPIB device messages categorized by function and also describes in detail these device messages arranged in alphabetical order, when the MU368030A Universal Modulation Unit installed with the MX368031A Device Test Signal Generation Software is mounted in the MG3681A Digital Modulation Signal Generator.

For further description of remote control, refer to Section 4 "Remote Control" in the MG3681A Main Unit Operation Manual.

5.1 List of Device Messages Categorized by Function

Command and query messages

The header portion of the command message is a reserved word represented by capital alphanumeric characters. The end of a query message header contains an interrogation mark (?). In the argument part of command and query messages, multiple arguments can be separated with a separator (,). Arguments are described below.

[1] Capitals : Reserved word

[2] Numerals : Reserved word

[3] Small letters in argument part:

f (Frequency) : Numeric data (NR1, NR2, NR3)

Suffix code : GHZ, GZ, MHz, MZ, kHz, KZ, HZ
When the unit is omitted, HZ is assumed.

l (level) (relative value) : Numeric data (NR1, NR2, NR3 format)

Suffix code : dB
When the unit is omitted, dB is assumed.

n (integer without unit) : Numeric data (NR1 format)

r (real number without unit) :
Numeric data (NR2 format)

h (hexadecimal number without unit) :
Numeric data (hexadecimal number)

s (character string) : Alphanumeric characters enclosed in double quotation marks (“ ”) or single quotation marks (‘ ’).

Device messages list

<Common>

Items	Device messages		
Control items	Command messages	Query messages	Response messages
I/Q Source Internal	MODE INT IQSRC INT	MODE? IQSRC?	MODE INT IQSRC INT
I/Q Source External	MODE EXT IQSRC EXT	MODE? IQSRC?	MODE EXT IQSRC EXT
I/Q Source OFF	MODE OFF IQSRC OFF	MODE? IQSRC?	MODE OFF IQSRC OFF
System DTSG	SYS DTSG	SYS?	SYS DTSG
Baseband ON	BASEBAND ON	BASEBAND?	BASEBAND ON
Baseband OFF	BASEBAND OFF	BASEBAND?	BASEBAND OFF
PM ON	PMO ON	PMO?	PMO ON
PM OFF	PMO OFF	PMO?	PMO OFF

<Modulation>

Items	Device messages		
Control items	Command messages	Query messages	Response messages
Pattern	PAT n n : 0 to 15	PAT?	PAT n
Reference Clock Source	REFCLK INT	REFCLK?	REFCLK INT
Reference Clock Source	REFCLK EXT	REFCLK?	REFCLK EXT
Reference Clock Source	REFCLK EXT2	REFCLK?	REFCLK EXT2
Start Trigger Delay	STDLY n n : 0 to 16777215	STDLY?	STDLY n
Start Trigger Source	STGS INT	STGS?	STGS INT
Start Trigger Source	STGS EXT	STGS?	STGS EXT

5.2 Details of Device Messages in Alphabetical Order

<Examples>

FREQ

Frequency

There is a space between a command message and “a”.

Function Sets the frequency.

Command message FREQ a

Entered value

Description of entered value

Value of a

Entered value		Description of entered value
–2.99975 to 3 GHZ	:	–2.99975 to 3 GHz
–2999.75 to 3000 MHZ	:	–2999.75 to 3000 MHz
–2999750 to 3000000 KHZ	:	–2999750 to 3000000 kHz
–2999750000.00 to 3000000000 HZ	:	–2999750000.00 to 3000000000 Hz

Query message FREQ?

Response message FREQ a

Example FREQ 123MHZ

BASEBAND

Baseband (On/Off)

Function Sets baseband On/Off.

Command message BASEBAND a

Value of a

ON	:	Baseband On
OFF	:	Baseband Off

Query message BASEBAND?

Response message BASEBAND a

Example BASEBAND ON

IQSRC

I/Q Source

Function	Selects the modulation source for digital modulation.
Command message	IQSRC a
Value of a	INT : Internal (internal modulation unit) EXT : External (external input) OFF : I/Q modulation stop (only pulse modulation enabled)
Query message	IQSRC?
Response message	IQSRC a
Example	IQSRC INT

PAT

Pattern

Function Selects the Device Test Signal.

Command message PAT n

Value of n 0 to 15

Query message PAT?

Response message PAT n,s

Restrictions For test signals associated with the value of "n," see "Device Test Signals list " in Section 3.1. Note that there may be some cases where there are fewer signals.

Example PAT 2

PMO

Pulse-Modulation

Function Sets On/Off and Internal/External of pulse modulation.

Command message PMO a

Value of a
INT : Internal (generates with modulation unit)
EXT : External (uses external device)
OFF : Off (signals always exist)

Query message PMO?

Response message PMO a

Example PMO ON

REFCLK

Reference Clock Source

Function Selects the baseband reference timing (external or internal).

Command message REFCLK a

Value of a

INT : Internal selection
EXT : External (TTL) selection
EXT2 : External 2 (AC: 5Vp-p) selection

Query message REFCLK?

Response message REFCLK a

Example REFCLK INT

STDLY

Start Trigger delay amount

Function	Sets the RF signal output timing.
Command message	STDLY n
Value of n	0 to 16777215
Query message	STDLY?
Response message	STDLY n
Restrictions	Only waveform data (such as 1xRTT Reverse) also allowing selection of external trigger can be set.
Example	STDLY 10

STGS

Start Trigger Source

Function	Sets On/Off and Internal/External of pulse modulation.
Command message	STGS a
Value of a	INT : Internal (generates with modulation unit) EXT : External (uses external device) OFF : Off (signals always exist)
Query message	STGS?
Response message	STGS a
Restrictions	Only waveform data (such as 1xRTT Reverse) also allowing selection of external trigger can be set.
Example	STGS INT

SYS

System

Function	Sets the digital modulation system.
Command message	SYS a
Value of a	NONE : Digital modulation system not mounted. DTSG : Device Test Signal Generation Software
Query message	SYS?
Response message	SYS a
Example	SYS DTSG

Section 6 Performance Test

This section describes the performance test when MX368031A Device Test Signal Generation Software is installed on the MU368030A Universal Modulation Unit, which is mounted on the MG3681A Digital Modulation Signal Generator. In order to implement the performance test as preventive maintenance, information such as required measuring instrument, setup procedure, and test procedures are included.

6.1 Performance Test

6.1.1 About the performance test

The performance test explained here is implemented as part of preventive maintenance against performance deterioration of the instrument. You are advised to implement a performance test whenever necessary, for examples, upon acceptance inspection, regular inspection, and post-repair performance confirmation. If you find an item, which does not meet specifications during a performance test, please contact Anritsu Corporation or one of our dealers.

The performance test consists of the following items:

- Modulation accuracy of RF output
- Waveform quality of RF output
- Output level accuracy

Be sure to implement periodically the performance test for items considered important as preventive maintenance. We recommend that the performance inspection is executed regularly once or twice a year.

In addition, it is recommended that the results are summarized using the Appendix C “Performance Test Record.”

CAUTION ⚠

Unless otherwise specified, be sure to warm up the device to be tested and the measuring instruments for at least 30 minutes or over until they become stable, before implementing the performance test. To ensure the maximum measurement accuracy, we recommend that you observe the above as well as keeping the room temperature, limiting AC power voltage fluctuations to a minimum, and making sure that there are no problems with noise, vibration, dust, humidity or other environmental factors.

6.1.2 Instruments required for the performance test

A list of instruments required for the performance test is shown below.

Test Item	Recommended Instrument	Anritsu Model Name
Modulation accuracy of RF output	Transmitter Tester (with GSM, π/4DQPSK analysis software)	MS8608A +MX860802A +MX860805A
Waveform quality of RF output	Transmitter Tester (with cdma analysis software)	MS8608A +MX860803A
Output level accuracy	Power meter Power sensor	ML4803A MA4601A

6.2 Modulation Accuracy of RF Output

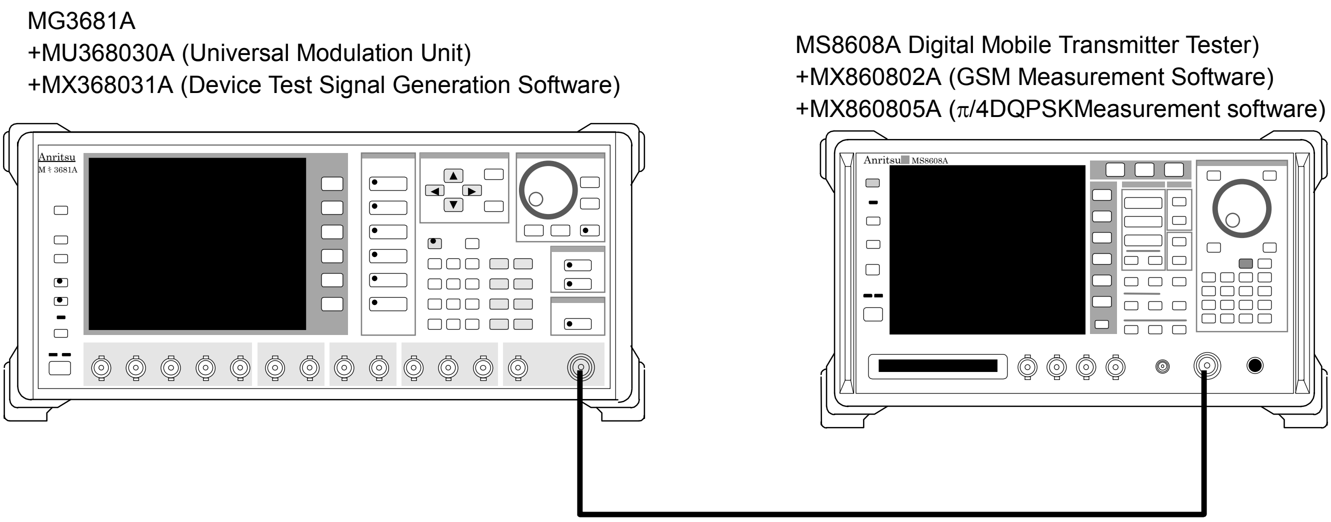
Test specifications

• EVM	≤ 1.8% (rms)
• PDC, PHS:	≤ 2.0% (rms)
• EDGE:	≤ 2.5% (rms)
• phase error	
GSM:	≤ 1°(rms) ≤ 3°(peak)

Conditions

RF output level	+5 dBm
Carrier frequency	100 to 2100 Hz
Level continuous mode	Off

Test procedures



[1] Set the modulation parameter of MG3681A as shown below:

Preset	: –
Baseband	: On
I/Q Mod	: Int
Digital Modulation	: On
System	: DTSG
Pattern	: Device Test Signal to be measured

[2] Set the frequency of MG3681A for the test frequency.

[3] Set +5dBm for the output level of MG3681A

[4] Set MS8608A for the setting of the modulation accuracy measurement. (Refer to the operation manual of MS8608A for details of the setting.)

[5] Measure the modulation accuracy of RF modulation signal using MS8608A.

6.3 Waveform Quality of RF Output

Test specifications

CDMA2000: ρ ≥ 0.997

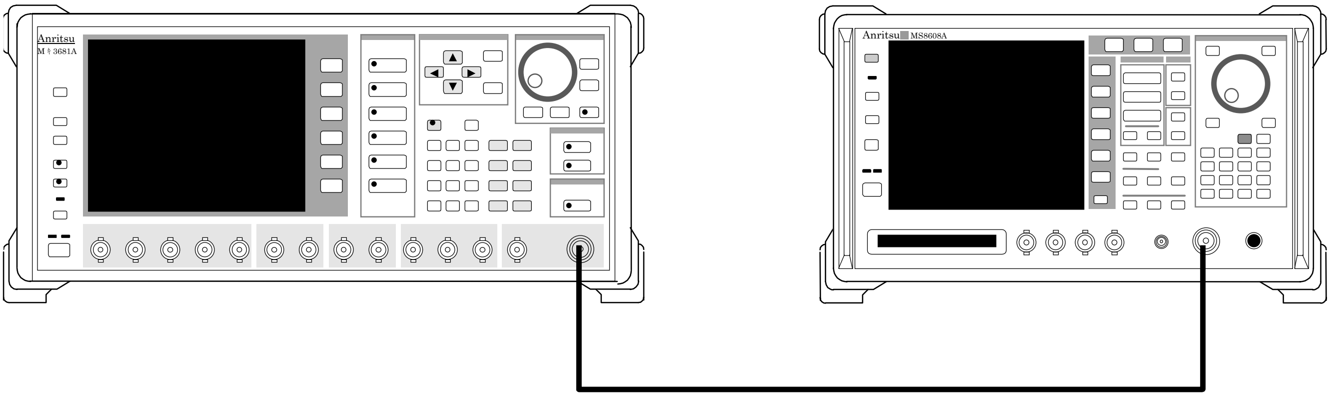
Conditions

RF output level	– 3 dBm
Carrier frequency	100 to 2300 MHz
Level continuous mode	Off

Test procedure

MG3681A
+ MU368030A(Universal Modulation Unit)
+ MX368031A（Device Test Signal Generation Software）

MS8608A Digital Mobile Transmitter Software
+MX860802A(GSM Measurement Software)
+MX860805A(π /4DQPSK Measurement Software)



[1] Set the modulation parameter of MG3681A as shown below:

Preset	: –
Baseband	: On
I/Q Mod	: Int
Digital Modulation	: On
System	: DTSG
Pattern	: Device Test Signal to be measured

[2] Set the frequency of MG3681A for the test frequency.

[3] Set -3 dBm for the output level of MG3681A.

[4] Set the MS8608A for the setting of the waveform quality measurement. (Refer to the operation manual of MS8608A for details of the setting.)

[5] Measure the waveform quality of RF output signal by using MS8608A.

6.4 Output Level Accuracy

Test specifications

Difference between the output levels in the CW mode and the followings.

PDC/PHS/IS-136	: ± 1.0 dB
GSM/EDGE	: ± 1.0 dB
CDMA2000 “RC1RVS/RC3RVS(1)“	: ± 1.0 dB
CDMA 2000 (others)	: ± 1.2 dB

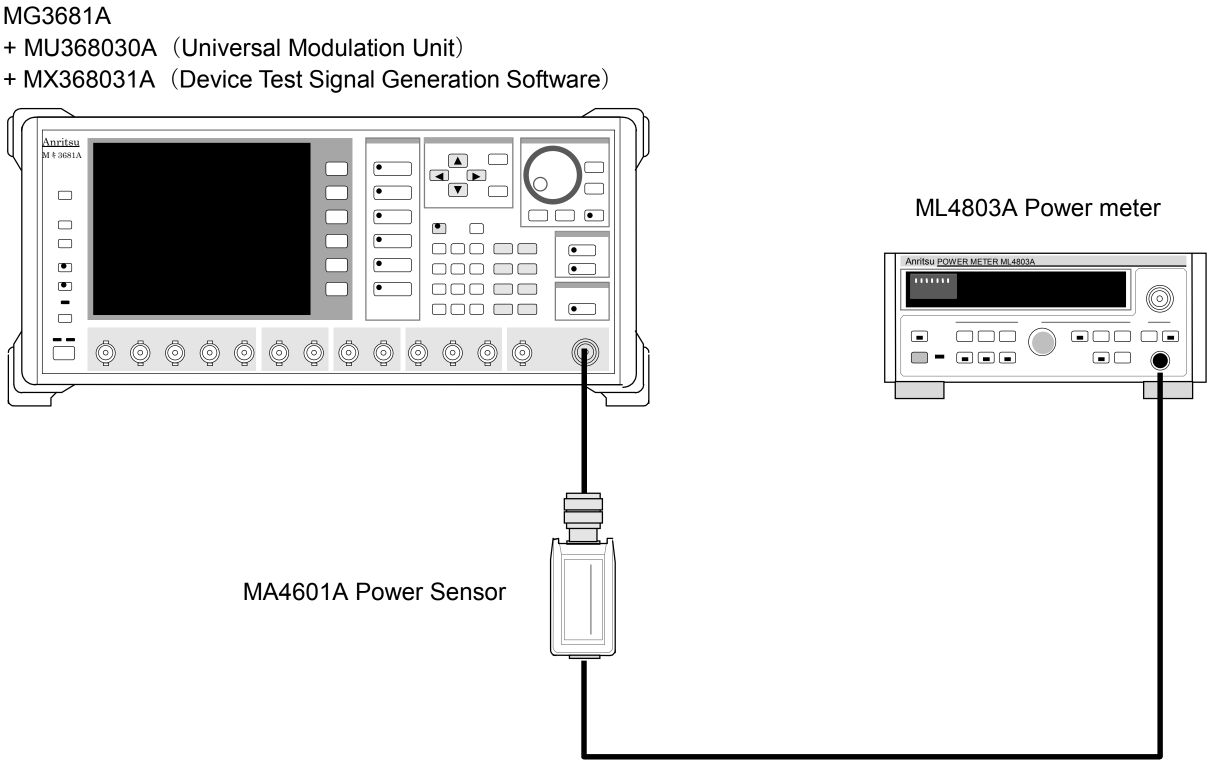
Conditions

RF output level

PDC/PHS/IS-136	: ≤ + 5 dBm
GSM/EDGE	: ≤ + 5 dBm
CDMA2000 “RC1RVS/RC3RVS(1)”	: ≤ – 3 dBm
CDMA2000 (Others)	: ≤ – 3 dBm

Carrier frequency	10 to 3000 MHz
Level continuous mode	Off

Test procedure



[1] Set the modulation parameter of MG3681A as shown below:

Preset	: –
Baseband	: On
I/Q Mod	: Int
Digital Modulation	: On
System	: DTSG
Pattern	: Device Test Signal to be measured

[2] Set RF output of MG3681A to Off.

[3] Execute the zero calibration and sensor sensitivity calibration of power meter

[4] Set the output level of MG3681A as desired. (Measurable low-level in the above system depends on the sensitivity of the power meter.)

[5] Set the calibration factor of power meter.

[6] Set the Digital Modulation of MG3681A to OFF, and measure the output level of MG3681A when CW is set.

[7] Set the Digital Modulation of MG3681A to ON, and measure the output level of MG3681A when modulation is in progress.

[8] Confirm whether the difference between the measured values obtained from step 6 and 7 is within the specifications.

Appendix

Appendix A Specifications

When installed in MU368030A mounted on MG3680 series

Item		Specifications
Corresponding System		EDGE, GSM, PDC, PHS, IS-136 CDMA2000（RC1 RVS, RC3 RVS, RC1-2 FWD, RC3-5 FWD, 1xEV-DO FWD, 1xEV-DO RVS）
Modulation System		EDGE :3π/8 offset 8PSK GSM :GMSK PDC, PHS, IS-136 : π/4 DQPSK CDMA2000 RC1 RVS :OQPSK CDMA2000 RC3 RVS :HPSK CDMA2000 RC1-2 FWD :BPSK CDMA2000 RC3-5 FWD :BPSK+QPSK 1xEV-DO FWD :16QAM 1xEV-DO RVS :BPSK
Baseband Filter		EDGE :Gauss Liner GSM :Gauss BbT=0.3 PDC, PHS :Root Nyquist α =0.5 IS-136 :Root Nyquist α=0.35 CDMA2000 RC1 RVS, RC3 RVS, 1xEV-DO RVS :IS-95spec CDMA2000 RC1-2 FWD, RC3-5 FWD, 1xEV-DO FWD :IS-95spec+EQ
Modulation Data		EDGE, GSM, PDC, PHS, IS-136 :PN9 continuous CDMA2000 :Depends on each channel configuration
Corresponding Channel Configuration	CDMA2000 RVS RC1	Corresponding Specifications 3GPP2 C.S0002-02 Channel configuration • Traffic Channel :Data Rate =9600 bps Long Code Mask = 0 Does not comply with MAC Layer.
	CDMA2000 RVS RC3(1)	Corresponding specifications 3GPP2 C.S0002-02 Channel configuration • Pilot Channel :Code Power – 5.278 dB • Fundamental Channel :Data Rate=9600 bps, Walsh Cover 4 Code Power – 1.528 dB Long Code Mask = 0 Does not comply with MAC Layer.
	CDMA2000 RVS RC3(2)	Corresponding specifications 3GPP2 C.S0002-02 Channel configuration • Pilot Channel :Code Power – 7.5912 dB • Fundamental Channel :Data Rate=9600 bps, Walsh Cover 4 Code Power – 3.8412 dB • Supplemental Channel :Data Rate=9600 bps, Walsh Cover 2 Code Power – 3.8412 dB Long Code Mask = 0 Does not comply with MAC Layer.

Item		Specifications
Corresponding Channel Configuration	CDMA2000 RVS RC3(3)	Corresponding specifications 3GPP2 C.S0002-02 Channel configuration • Pilot Channel :Code Power – 5.278 dB • Dedicated Control Channel :Data Rate=9600 bps, Walsh Cover 8 Code Power – 1.528 dB Long Code Mask = 0 Does not comply with MAC Layer.
	CDMA2000 FWD RC1-2	Corresponding specifications 3GPP2 C.S0002-02 Channel configurations • Pilot Channel :Code Power – 7.0 dB • Sync Channel :BPSK , Symbol Rate=4.8 ksps Walsh Cover 32, Code Power – 13.3 dB • Paging Channel :BPSK , Symbol Rate=19.2 ksps Walsh Cover 1, Code Power – 7.3 dB • Traffic Channel :BPSK , Symbol Rate=19.2 ksps Walsh Cover 8-13, Code Power –10.3 dB Long Code Mask = 0 Does not comply with TPC MUX. Does not comply with Channel Coding
	CDMA2000 FWD RC3-5	Corresponding specifications 3GPP2 C.S0002-02 Channel configuration • Pilot Channel :Code Power – 7.0 dB • Sync Channel :BPSK, Symbol Rate=4.8 ksps Walsh Cover 32, Code Power – 13.3 dB • Paging Channel :BPSK, Symbol Rate=19.2 ksps Walsh Cover 1, Code Power – 7.3 dB • Traffic Channel :QPSK, Symbol Rate=38.4 ksps Walsh Cover 8-13, Code Power –10.3 dB Long Code Mask = 0 Does not comply with TPC MUX. Does not comply with Channel Coding
	1xEV-DO FWD	Corresponding specifications 3GPP2 C.S0024 Version 2.0 Channel configuration : • Priamble :MACindex=5 • Pilot Channel: • MAC Channel :RPC bit All"0", MAC index=5, Power = – 3 dB RA bit All"0", Power = – 3 dB • Traffic Channel :16QAM, 1536 symbol / slot (Data is PN15) Does not comply with Channel Coding, and modulates 6144-bit / slot of PN15 directly by 16QAM modulation. Time-Division Multiplexing :1-Slot Case

<table>
<tr><th colspan="2">Item</th><th>Specifications</th></tr>
<tr><td>Corresponding Channel Configuration</td><td>1xEV-DO
RVS</td><td>Corresponding specifications 3GPP2 C.S0024 Version 2.0
Channel configuration
• Pilot Channel :Code Power = – 18.68 dB
• MAC Channel :RRI Symbol “101”, Code Power = – 18.68 dB
DRC Symbols “01(h)” All slots are Active,
Code Power = – 18.68 dB
DRC Cover Symbols “0”
• ACK Channel :All”0” All slots are Active, Code Power = – 18.68 dB
• Data Channel :Symbol Rate=307.2 ksps, Code Power = – 0.18 dB
Does not comply with Channel Coding
Long Code Mask :MI=3FFFFFFFFFF(h), MQ=00000000001(h)</td></tr>
<tr><td rowspan="4">RF Out-put</td><td>Carrier Frequency Range</td><td>10 to 3000 MHz</td></tr>
<tr><td>Output
Level
Accuracy</td><td>For output level when CW is set:
• PDC, PHS, IS-136 : ± 1.0 dB (at ≤ +5 dBm)
• GSM, EDGE : ± 1.0 dB (at ≤ +5 dBm)
• CDMA2000 RC1 RVS, RC3 RVS(1) : ± 1.0 dB (at ≤ – 3 dBm)
• CDMA2000 RC3 RVS(2,3) RC1-2 FWD, RC3-5 FWD, 1xEV-DO
: ± 1.2 dB (at ≤ – 3 dBm)</td></tr>
<tr><td>Modulation
Accuracy</td><td>When +5 dBm is output in the range from 100 to 2100 MHz
EVM
• PDC, PHS :1.8%(rms)
• IS-136 :2.0%(rms)
• EDGE :2.5%(rms)
Phase Error
• GSM :1°(rms), 3° (peak) (at 18 to35°C)</td></tr>
<tr><td>Waveform
Quality</td><td>When –3 dBm is output in the range from 100 to 2300 MHz, and from 18 to 35°C.
CDMA2000（1xEV-DO excluded.） : ρ ≥ 0.997</td></tr>
</table>

<table>
<tr><th colspan="2">Item</th><th>Specifications</th></tr>
<tr><td rowspan="2">RF Out-put</td><td>Leakage Power Adjacent Channel</td><td>RF output level:+5 dBm, detection mode: at POSITIVE PEAK
• PDC (PLL MODE :NORMAL, 100 to 1600 MHz, RBW1 kHz, VBW 3 kHz)
≤ – 63 dBc (50 kHz offset, 21 kHz BW)
≤ – 67 dBc (100 kHz offset, 21 kHz BW)

• PHS (PLL MODE:NARROW, 100 to 1000 MHz,1750 to 2500 MHz, RBW 3 kHz,VBW 10 kHz)
≤ – 66 dBc (600 kHz offset, 192 kHz BW)
≤ – 69 dBc (900 kHz offset, 192 kHz BW)

• IS-136 (PLL MODE:NORMAL, 100 to 2100 MHz, RBW 1 kHz, VBW 3kHz)
≤ – 42 dBc (30 kHz offset, 24.3 kHz BW)
≤ – 64 dBc (60 kHz offset, 24.3 kHz BW)
≤ – 64 dBc (90 kHz offset, 24.3 kHz BW)

• GSM (PLL MODE:NARROW, 100 to 3000 MHz, RBW3 kHz, VBW 10 kHz)
≤ – 35 dBc (200 kHz offset, 30 kHz BW)
≤ – 66 dBc (400 kHz offset, 30 kHz BW)

• EDGE (PLL MODE:NARROW, 100 to 3000 MHz, RBW3 kHz, VBW 10 kHz)
≤ – 38 dBc (200 kHz offset, 30 kHz BW)
≤ – 67 dBc (400 kHz offset, 30 kHz BW)

Note that performance deterioration of MG3681A caused by Spurious is excluded.</td></tr>
<tr><td>Spurious Emission</td><td>In the range from 100 to 2300 MHz, ratio of total power to power within 30 kHz band at –3 dBm output
When PLL MODE:NORMAL is set

• CDMA2000 RC1-2 FWD
≤ – 62 dBc (885 kHz ≤ offset < 1.98 MHz)
≤ – 67 dBc (1.98 MHz ≤ offset < 2.5 MHz)
≤ – 77 dBc (2.5 MHz ≤ offset < 5.0 MHz)

• CDMA2000, others
≤ – 65 dBc (885 kHz ≤ offset < 1.98 MHz)
≤ – 70 dBc (1.98 MHz ≤ offset < 2.5 MHz)
≤ – 77 dBc (2.5 MHz ≤ offset < 5.0 MHz)

Note that performance deterioration of MG3681A caused by Spurious is excluded.</td></tr>
</table>

Item		Specifications
IQ Out-put	IQ Output Level	PDC, PHS, IS-136 :359 mV(rms) GSM :357 mV(rms) EDGE :287 mV(rms) CDMA2000 RC1RVS :287 mV(rms) CDMA2000 RC3RVS :203 mV(rms) CDMA2000 FWD :101 mV(rms) 1xEV-DO :101 mV(rms)
	IQ Output Level	± 5% (OPT-11 not mounted) ± 10% (OPT-11 mounted)
Setting range of Level Continuos Mode		+10 to – 10 dB
Transmission Speed	Symbol Rate	PDC :21 ksps PHS :192 ksps IS-136 :12.15 ksps GSM :270.833 ksps EDGE :270.833 ksps
	Chip Rate	CDMA2000 :1.2288Mcps
	Transmission Speed Accuracy	Depends on reference signal accuracy of MG 3680 series (Excluded in external synchronization)
	Backup Area of Firmware Used	CPU:137.3 kByte, FPGA:49.5 kByte

Appendix B List of Initial Value

Setting	Initial Value
Digital Modulation Main Screen	
Pattern	0:GSM_EDGE
Trigger Source	Int
Trigger Delay	0/48sps (0.0000sps)
Reference Clock	Int

Appendix C Performance Test Record

Tested at:________________________________ Report No. ________________

____________________________ Date ________________

____________________________ Tested by ________________

Product Name MG3681A Digital Modulation SG
+MU368030A Universal Modulation Unit
+MX368031A Device Test Signal Generator Software

Serial No. ________________ Ambient temperature ________°C
AC Power frequency ________Hz Relative Humidity ________%

Remarks:

____

____

____

____

Modulation Accuracy (Section 6.2)

- EVM

Device Test Signal	Setting Output Level	Result					Specifi-cations Maximum
		MHz	MHz	MHz	MHz	MHz	
PDC	+5 dBm						1.8%
PHS	+5 dBm						1.8%
IS-136	+5 dBm						2.0%
EDGE	+5 dBm						2.5%

- Phase Error

Device Test Signal	Setting Output Level	Result					Specifi-cations Maximum
		MHz	MHz	MHz	MHz	MHz	
GSM	+5 dBm						1° (rms)
							3° (peak)

Waveform (Section 6.3)

Device Test Signal	Setting Output Level	Result					Specifications Minimum
		MHz	MHz	MHz	MHz	MHz	
RC1 RVS	– 3 dBm						0.997
RC3 RVS(1)	– 3 dBm						0.997
RC3 RVS(2)	– 3 dBm						0.997
RC3 RVS(3)	– 3 dBm						0.997
RC1-2 FWD	– 3 dBm						0.997
RC3-5 FWD	– 3 dBm						0.997

Output Level Accuracy (Section 6.4)

Device Test Signal	Setting Output Level	Result					Specifi-cations Maximum
		MHz	MHz	MHz	MHz	MHz	
PDC	dBm						± 1.0 dB
PHS	dBm						± 1.0 dB
IS-136	dBm						± 1.0 dB
GSM	dBm						± 1.0 dB
EDGE	dBm						± 1.0 dB
RC1 RVS	dBm						± 1.0 dB
RC3 RVS(1)	dBm						± 1.0 dB
RC3 RVS(2)	dBm						± 1.2 dB
RC3 RVS(3)	dBm						± 1.2 dB
RC1-2 FWD	dBm						± 1.2 dB
RC3-5 FWD	dBm						± 1.2 dB
1xEV-DO FWD	dBm						± 1.2 dB
1xEV-DO RVS	dBm						± 1.2 dB

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